A New Control Method to Reduce Parasitic Losses in a Ring-Type DC-DC Converter

Kei Eguchi and Ichirou Oota

***Abstract*—A ring-type converter is one of the efficient step-up/step-down DC-DC converters, because the ring-type converter can be implemented using semiconductor switches and capacitor. In this paper, a ring-type DC-DC converter using charge reusing techniques is proposed to improve power efficiency. Although the conventional ring-type converter consumes the electric charge in stray parasitic capacitances idly, the proposed converter reuses a part of the electric charge in stray parasitic capacitances. Therefore, the proposed converter can realize higher power efficiency than the conventional ring-type converter, because the proposed converter can reduce parasitic power losses. Concerning the proposed converter with three capacitors, simulation program with integrated circuit emphasis (SPICE) simulations and theoretical analysis were performed to clarify characteristics. The result of SPICE simulations showed that more than 8.2% of the power efficiency was improved by the proposed converter when the output load is 10kΩ. Furthermore, handy theoretical equations to estimate the maximum efficiency were obtained by the theoretical analysis.**

***Index Terms*—Charge reusing techniques, DC-DC converters, step-up/step-down conversion, switched capacitor circuits.**

I. Introduction

In the development of mobile devices, the switched capacitor (SC) power converter [1]-[18] is one of the most promising converters, because the SC power converter can be implemented into an integrated circuit (IC) chip. For example, Doms et al. designed a capacitive power management circuit by using charge pumps [1], Kim realized white light emitting diode (WLED) backlights using a negative charge pump [2], and Ishida et al. proposed non-volatile memories using a positive/negative charge pump [3]. Furthermore, SC power converters came to be used for a building block of energy harvesting applications in recent years [4], [5]. For these application systems, several kinds of SC circuit topologies have been proposed in past studies: charge-pump circuits [1]-[6], series-parallel type converters [7], Fibonacci-type converter [8], and so on. Among others, the ring-type converter [9]-[13] is the unique converter which can achieve step-up/step-down conversion.

In the design of DC-DC converters, improving power efficiency is one of the most important issues, because cooling of inefficient power converters is difficult and expensive. The power efficiency of the SC DC-DC converter consisting of discrete components is mainly limited by capacitor charging and discharging losses and resistive conduction losses. However, the energy loss due to stray parasitic capacitances cannot be ignored in the integrated circuit (IC) design of the SC converters. For this reason, several techniques have been proposed to reduce parasitic power losses [14]-[18]. For example, Lauterbach *et al.* proposed charge sharing concept and new clocking scheme for the power efficiency improvement of boosted charge pumps [15], where the combination of tristate drivers and a new clocking scheme eliminates parasitic charge current peaks. Furthermore, Allasasmeh *et al*. applied a charge reusing technique to not only the charge pump circuit but also a heap converters and a Fibonacci converter [17], where two symmetrical converter blocks are operated in parallel by using complementary control signals. However, concerning a ring-type converter, energy loss due to stray parasitic capacitances has not been taken into account in previous studies [9]-[12].

In this paper, a ring-type DC-DC converter using charge reusing techniques is proposed to improve power efficiency. Unlike the conventional converter [9]-[12], the proposed converter reuses a part of the electric charge in stray parasitic capacitances by connecting stray parasitic capacitances at the end of each clock cycle. By alleviating parasitic power losses, the proposed converter can achieve higher power efficiency than the conventional converter. To confirm the validity of the proposed converter, simulation program with integrated circuit emphasis (SPICE) simulations are performed.

II. Circuit Structure

A. Conventional Ring-Type Converter

Fig. 1 shows the conventional ring-type converter [9]-[12]. The conventional converter consists of $4N$ (N=1, 2…) power switches and N capacitors. By controlling power switches, the conventional converter realizes s/r ((r=1, 2... N) and (s = 1,2, …, N)) step-up/step-down conversion. In Fig.1, clock pulses for the power switch $S_{1,j}$ (j=1,2,... , N) are non-overlapped N-phase pulses $\Phi_{1,j}$ and clock pulses for $S_{2,j}$ are set to inverted pulses of $\Phi_{1,j}$. According to the conversion ratio s/r, the power switches $S_{3,j}$ and $S_{4,j}$ are driven by clock pulses obtained by shifting the clock pulse $\Phi_{1,j}$ cyclically. In other words, by controlling the timing of $\Phi_{3,j}$ and $\Phi_{4,j}$, the conversion ratio is determined. Concretely, in the case of N=3, the timing of the clock pulses in the case of 3x step-up conversion as shown in Table I.

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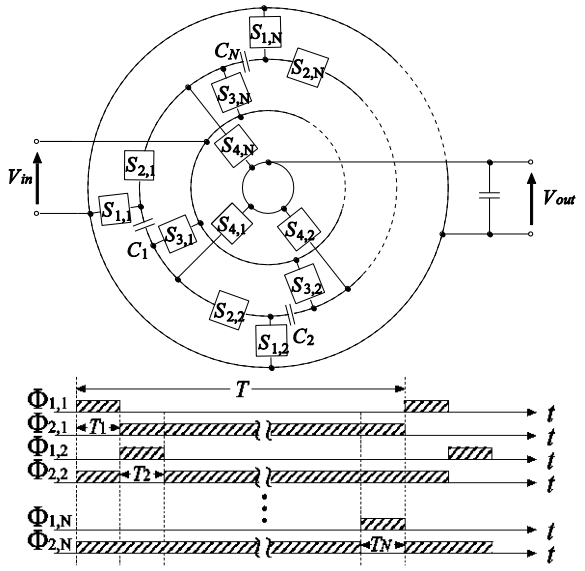


Fig. 1. Conventional ring-type converter.

TABLE I: TIMING OF CLOCK PULSES IN THE CASE OF 3X STEP-UP

3x step-up	On	Off
State-T_1	$S_{1,1}$, $S_{2,2}$, $S_{2,3}$, $S_{3,1}$, $S_{4,3}$	Other switches
State-T_2	$S_{1,2}$, $S_{2,3}$, $S_{2,1}$, $S_{3,2}$, $S_{4,1}$	Other switches
State-T_3	$S_{1,3}$, $S_{2,1}$, $S_{2,2}$, $S_{3,3}$, $S_{4,2}$	Other switches

In the previous studies [9]-[12], the existence of stray parasitic capacitances has not been taken into account in the design of the ring-type converter. When the SC DC-DC converter is integrated into an IC form, stray parasitic capacitances exist as shown in Fig. 2, where C_t denotes the stray parasitic capacitance between top plate and substrate and C_b denotes the stray parasitic capacitance between bottom plate and substrate. In the conventional converter, the electric charge Q charged in C_b is consumed idly when C_j (j=1, 2..., N) is grounded via $S_{1,j}$.

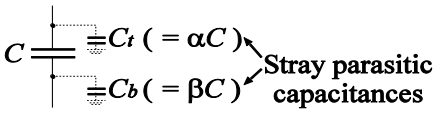


Fig. 2. Stray parasitic capacitances.

B. Proposed Converter

Fig. 3 shows the proposed converter. In Fig. 3, C_j (j=1, 2, …, N) is the capacitor, C_{tj} (=αC_j) denotes the j-th stray parasitic capacitance between top plate and substrate, and C_{bj} (=βC_j) denotes the j-th stray parasitic capacitance between bottom plate and substrate. The proposed converter consists of 5N power switches and N capacitors. Unlike the conventional ring-type DC-DC converter [9]-[12], the capacitor C_j of the proposed converter is connected each other through the power switch $S_{5,j}$.

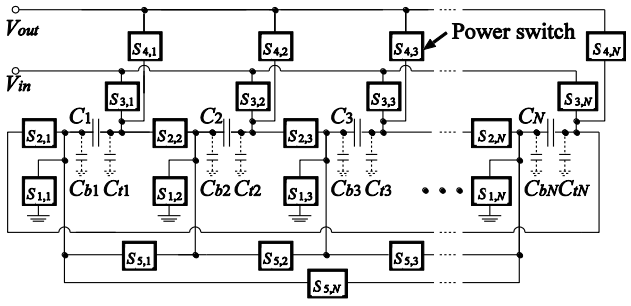


Fig. 3. Proposed ring-type converter.

To help readers' understanding, let us consider the proposed converter in the case of N=3. Table II shows the timing of the clock pulses in the case of 2/3x step-down conversion. Unlike the conventional converter, the proposed converter is controlled by 2N-phase clock pulses. As Table II shows, the power switch $S_{5,k}$ (k = {1, 2, 3}) is turned on at the end of each clock cycle. In State-T_2, State-T_4 and State-T_6, the electric charges stored in C_{bk} (k = {1, 2, 3}) are equalized through the power switch $S_{5,k}$ before the electric charges are consumed idly. In other words, the power dissipation of the input can be reduced by the equalization process. Therefore, due to the equalization process of the electric charge in C_{bk}, the power dissipation of the input can be reduced.

TABLE II: TIMING OF CLOCK PULSES IN THE CASE OF 2/3X STEP-DOWN

2/3x step-down	On	Off
State-T_1	$S_{1,1}$, $S_{2,2}$, $S_{2,3}$, $S_{3,3}$, $S_{4,2}$	Other switches
State-T_2	$S_{5,1}$	Other switches
State-T_3	$S_{1,2}$, $S_{2,3}$, $S_{2,1}$, $S_{3,1}$, $S_{4,3}$	Other switches
State-T_4	$S_{5,2}$	Other switches
State-T_5	$S_{1,3}$, $S_{2,1}$, $S_{2,2}$, $S_{3,2}$, $S_{4,1}$	Other switches
State-T_6	$S_{5,3}$	Other switches

III. THEORETICAL ANALYSIS

Concerning power efficiency and output voltage, the theoretical analysis is performed in this section. To evaluate the maximum power efficiency and the maximum output voltage, we assume that 1. Parasitic elements are negligibly small and 2. Time constant is much larger than the period of clock pulses.

A. Step-Down Conversion

Fig. 4 shows the instantaneous equivalent circuits of the proposed converter in the case of the step-down conversion, where R_{on} denotes the on-resistance of the power switch. In Fig. 4, State-T_k (k=1, 3,…, 2N-1) is the charging and transferring process and State-T_l (l=2, 4, …, 2N) is the charge reusing process, where k is an odd number and l is an even number. In Fig. 4, the differential value of the electric charge in capacitor C_n (n=1, 2,.., N) satisfies

$$\sum_{i=1}^{2N} \Delta q_{T_i}^{n} = 0 \tag{1}$$

where $T = \sum_{i=1}^{2N} T_i$, $T_k = T_a$, and $T_l = \gamma T$.

In (1), γ(<0.5) is a constant parameter, T_a is a time for the charging and transferring process, and $\Delta q_{Ti}^{\ n}$ (i=1, 2, …, 2N) denotes electric charges in the case of *State*-T_i.

In the case of *State*- T_k, the differential values of electric charges in the terminal V_{in} and terminal V_{out}, $\Delta q_{Tk,Vin}$ and $\Delta q_{Tk,Vout}$, are expressed by the following equations:

$$\Delta q_{T_k,V_{in}} = \Delta q_{T_k}^{u}$$

and

$$\Delta q_{T_k,V_{out}} = -\Delta q_{T_k}^{u} + \Delta q_{T_k}^{v} \tag{2}$$

where $u = \begin{cases} (k-1)/2 + r & \text{if } (k-1)/2 + r \le N \\ (k-1)/2 + r - N & \text{if } (k-1)/2 + r > N \end{cases}$

and

$$v=\begin{cases}(k-1)/2+s & if \quad (k-1)/2+s\le N\\ (k-1)/2+s-N & if \quad (k-1)/2+s>N\end{cases}$$

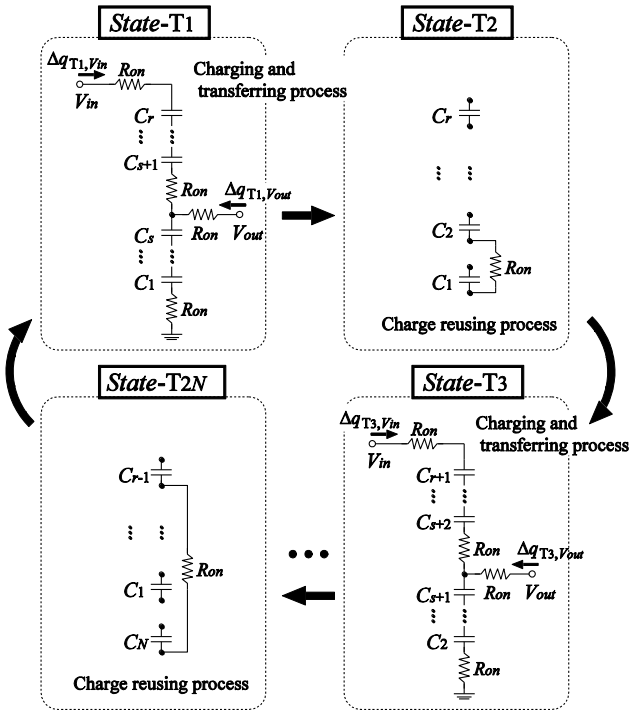


Fig. 4. Instantaneous equivalent circuit in the case of the step-down conversion.

Furthermore, in *State*- T_k (k=1, 3, …, 2N-1), the following conditions are satisfied:

$$\Delta q_{T_k}^{(k+1)/2}=\cdots=\Delta q_{T_k}^{v}$$

$$\Delta q_{T_k}^{u}=\cdots=\Delta q_{T_k}^{w}$$

and

$$\Delta q_{T_k}^{N+1}=\cdots=\Delta q_{T_k}^{2N}=0 \tag{3}$$

where

$$w=\begin{cases}v+1 & if \quad v+1\le N\\ (v+1)-N & if \quad v+1>N\end{cases}$$

On the other hand, the differential values of electric charges in the case of *State*- T_l (l=2, 4, …, 2N) is as follows:

$$\Delta q_{T_l,V_{in}}=0$$

and

$$\Delta q_{T_l,V_{out}}=0 \tag{4}$$

Using (2)-(4), the average input current is expressed as

$$\overline{I_{in}}=\sum_{i=1}^{2N}\frac{\Delta q_{T_i,V_{in}}}{T}=\sum_{k=1}^{2N-1}\frac{\Delta q_{T_k}^{u}}{T} \tag{5}$$

From (1)-(4), the average input current (5) can be rewritten as

$$T\overline{I_{out}}=-T\overline{I_{in}}+N\Delta q_{T_1}^{1} \tag{6}$$

On the other hand, the average output current is expressed as

$$\overline{I_{out}}=\sum_{i=1}^{2N}\frac{\Delta q_{T_i,V_{out}}}{T}=\sum_{k=1}^{2N-1}\frac{\left(-\Delta q_{T_k}^{u}+\Delta q_{T_k}^{v}\right)}{T} \tag{7}$$

From (1)-(4), the average output current (7) can be rewritten as

$$\overline{I_{out}}=\frac{Nr}{(r-s)T}\Delta q_{T_1}^{1} \tag{8}$$

Substituting (6) into (8), we have the following relation between the average output current and the average input current:

$$\overline{I_{in}}=-\left(\frac{s}{r}\right)\overline{I_{out}} \tag{9}$$

Next, let us consider the consumed energy in one period. In Fig. 4, the consumed energy in one period can be expressed as

$$W_T=\sum_{i=1}^{2N}W_{T_i}=NW_{T_1}, \tag{10}$$

where

$$W_{T_1}=\frac{(r-s+1)R_{on}}{T_a}\left(\Delta q_{T_1}^{r}\right)^2+\frac{sR_{on}}{T_a}\left(\Delta q_{T_1}^{1}\right)^2+\frac{R_{on}}{T_a}\left(\Delta q_{T_1}^{1}-\Delta q_{T_1}^{r}\right)^2$$

Using (1)-(4), the consumed energy (10) can be rewritten as

$$W_T=\frac{NR_{on}}{T_a}\left(\Delta q_{T_1}^{1}\right)^2\left\{\frac{s^2(r-s+1)}{(r-s)^2}+\frac{s(r-s)^2}{(r-s)^2}+\frac{r^2}{(r-s)^2}\right\} \tag{11}$$

Here, it is known that a general equivalent circuit of SC DC-DC converters can be expressed by the circuit shown in Fig. 5 [12]-[14], where R_{SC} is called the SC resistance and m is a ratio of the ideal transformer. In the general equivalent circuit of SC DD-DC converters, the consumed energy W_T is defined by

$$W_T:=\left(\overline{I_{out}}\right)^2\cdot R_{SC}\cdot T=\left(\frac{\Delta q_{out}}{T}\right)^2\cdot R_{SC}\cdot T \tag{12}$$

where R_{SC} is called the SC resistance. Therefore, from (8), (11), and (12), the SC resistance in the case of the step-down conversion is expressed as

$$R_{SC}=R_{on}\left\{\frac{s^2(r-s+1)+s(r-s)^2+r^2}{r^2(1-\gamma N)}\right\} \tag{13}$$

By combining (9) and (13), the equivalent circuit in the case of the step-down conversion can be expressed by the following determinant:

$$\begin{bmatrix}\overline{V_{in}}\\ \overline{I_{in}}\end{bmatrix}=\begin{bmatrix}r/s & 0\\ 0 & s/r\end{bmatrix}\begin{bmatrix}1 & R_{SC}\\ 0 & 1\end{bmatrix}\begin{bmatrix}\overline{V_{out}}\\ -\overline{I_{out}}\end{bmatrix}, \tag{14}$$

Because the equivalent circuit of the SC DC-DC converters can be expressed by the determinant using the Kettenmatrix. Finally, from (14), the power efficiency and the output voltage of the proposed converter are obtained as

$$\eta=\frac{\left(\overline{I_{out}}\right)^2R_L}{\left(\overline{I_{out}}\right)^2R_{SC}+\left(\overline{I_{out}}\right)^2R_L}=\frac{R_L}{R_{SC}+R_L}$$

and

$$V_{out}=\frac{R_L}{R_{SC}+R_L}\times\left(\frac{s}{r}\right)V_{in}, \tag{15}$$

where R_L denotes the output load. As (13) and (15) show, the power efficiency decreases with increase in R_{on} and γ.

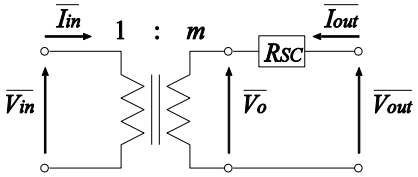


Fig. 5. General equivalent circuit of the SC power converter.

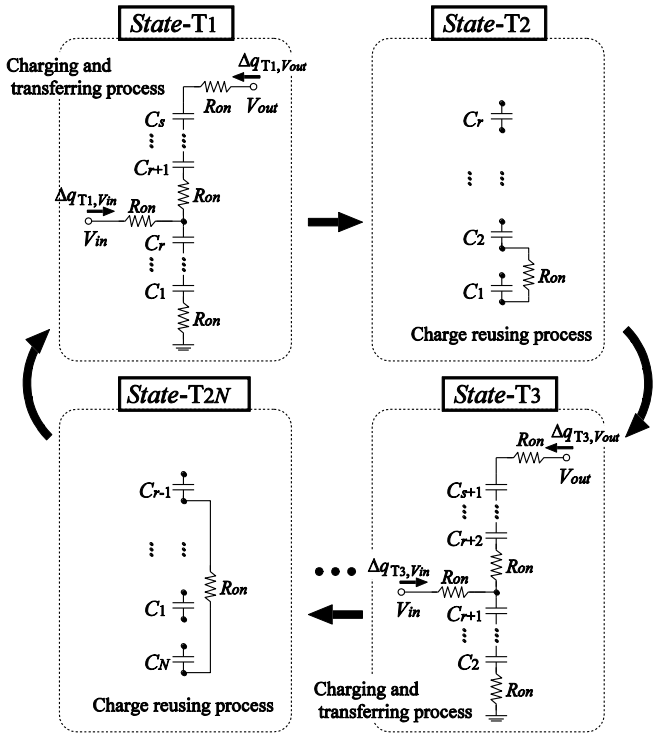


Fig. 6. Instantaneous equivalent circuit in the case of the step-up conversion.

B. Step-Up Conversion

Fig. 6 shows the instantaneous equivalent circuits of the proposed converter in the case of the step-up conversion. In the case of *State-* T_k (k=1, 3, …, 2N-1), the differential values of electric charges in the terminal V_{in} and terminal V_{out}, $\Delta q_{Tk,Vin}$ and $\Delta q_{Tk,Vout}$, are expressed by the following equations:

$$\Delta q_{T_k,V_{in}} = \Delta q_{T_k}^{u} - \Delta q_{T_k}^{v}$$

and

$$\Delta q_{T_k,V_{out}} = \Delta q_{T_k}^{v}, \tag{16}$$

where

$$u = \begin{cases} (k-1)/2 + r & if \quad (k-1)/2 + r \le N \\ (k-1)/2 + r - N & if \quad (k-1)/2 + r > N \end{cases}$$

and

$$v = \begin{cases} (k-1)/2 + s & if \quad (k-1)/2 + s \le N \\ (k-1)/2 + s - N & if \quad (k-1)/2 + s > N. \end{cases}$$

Furthermore, in *State-*T_k, the following conditions are satisfied:

$$\Delta q_{T_k}^{(k+1)/2} = \cdots = \Delta q_{T_k}^{u},$$

$$\Delta q_{T_k}^{v} = \cdots = \Delta q_{T_k}^{p},$$

and

$$\Delta q_{T_k}^{N+1} = \cdots = \Delta q_{T_k}^{2N} = 0, \tag{17}$$

where

$$p = \begin{cases} u+1 & if \quad u+1 \le N \\ (u+1) - N & if \quad u+1 > N. \end{cases}$$

On the other hand, the differential values of electric charges in the case of *State-* T_l (l=2, 4, …, 2N) is as follows:

$$\Delta q_{T_l,V_{in}} = 0$$

and

$$\Delta q_{T_l,V_{out}} = 0 \tag{18}$$

Using (16) - (18), the average input current is expressed as

$$\overline{I_{in}} = \sum_{i=1}^{2N} \frac{\Delta q_{T_i,V_{in}}}{T} = \sum_{k=1}^{2N-1} \frac{\left(\Delta q_{T_k}^{u} - \Delta q_{T_k}^{v}\right)}{T} \tag{19}$$

From (1), (16)-(18), the average input current (19) can be rewritten as

$$T\overline{I_{in}} = -T\overline{I_{out}} + N\Delta q_{T_1}^{1} \tag{20}$$

On the other hand, the average output current is expressed as

$$\overline{I_{out}} = \sum_{i=1}^{2N} \frac{\Delta q_{T_i,V_{out}}}{T} = \sum_{k=1}^{2N-1} \frac{\Delta q_{T_k}^{v}}{T} \tag{21}$$

From (1), (16)-(18), the average output current (21) can be rewritten as

$$\overline{I_{out}} = \frac{Nr}{(r-s)T} \Delta q_{T_1}^{1} \tag{22}$$

Substituting (20) into (22), the relation between the average output current and the average input current can be obtained by (9).

Next, in the case of the step-up conversion, the consumed energy can be expressed as

$$W_T = \sum_{i=1}^{2N} W_{T_i} = NW_{T_1}, \tag{23}$$

where

$$W_{T_1} = \frac{(s-r+1)R_{on}}{T_a}\left(\Delta q_{T_1}^{s}\right)^2 + \frac{rR_{on}}{T_a}\left(\Delta q_{T_1}^{1}\right)^2 + \frac{R_{on}}{T_a}\left(\Delta q_{T_1}^{1} - \Delta q_{T_1}^{s}\right)^2$$

Using (1), (16)-(18), the consumed energy (23) can be rewritten as

$$W_T = \frac{NR_{on}}{T_a}\left(\Delta q_{T_1}^{1}\right)^2 \left\{ \frac{r^2(s-r+1)}{(s-r)^2} + \frac{r(s-r)^2}{(s-r)^2} + \frac{s^2}{(s-r)^2} \right\} \tag{24}$$

Therefore, from (12), (22), and (24), the SC resistance in the case of the step-up conversion is expressed as

$$R_{SC} = R_{on} \left\{ \frac{r^2(s-r+1) + r(s-r)^2 + s^2}{r^2(1-\gamma N)} \right\} \tag{25}$$

By combining (9) and (25), the equivalent circuit in the case of the step-up conversion can be expressed by (14).

C. Design Condition for Charge Reusing Process

From [12], the maximum power efficiency of the conventional ring-type converter is given by (15), where the SC resistance of the conventional converter, R_{SCC}, is expressed as

Step-down conversion:

$$R_{SCC} = R_{on}\left\{\frac{s^2(r-s+1)+s(r-s)^2+r^2}{r^2}\right\} \quad (26)$$

Step-up conversion:

$$R_{SCC} = R_{on}\left\{\frac{r^2(s-r+1)+r(s-r)^2+s^2}{r^2}\right\} \quad (27)$$

From (13), (25), (26), and (27), the ratio of the SC resistances between the conventional converter and the proposed converter, R_{SCC}/R_{SC}, is expressed by

Step-down conversion:

$$\frac{R_{SCC}}{R_{SC}} = 1-\gamma N \quad (28)$$

Step-up conversion:

$$\frac{R_{SCC}}{R_{SC}} = 1-\gamma N \quad (29)$$

As (28) and (29) show, is it desirable for the parameter γ to satisfy $1>>\gamma N$.

IV. Simulation

Concerning the proposed converter in the case of N=3, the SPICE simulation is performed to investigate the properties of the proposed converter. Fig. 7 shows the proposed ring-type converter in the case of N=3. The conditions for the SPICE simulation are as follows: V_{in}=3.7V, $C_1 = C_2 = C_3$ = 20nF, R_{on}=10Ω, T=150ns, T_a=45ns, and γ=1/30. In the SPICE simulation, C_{tj} and C_{bj} were assumed to be the same value, because the value of the stray parasitic capacitance changes according to a semiconductor process.

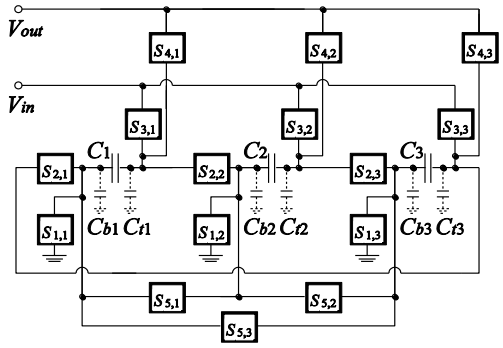
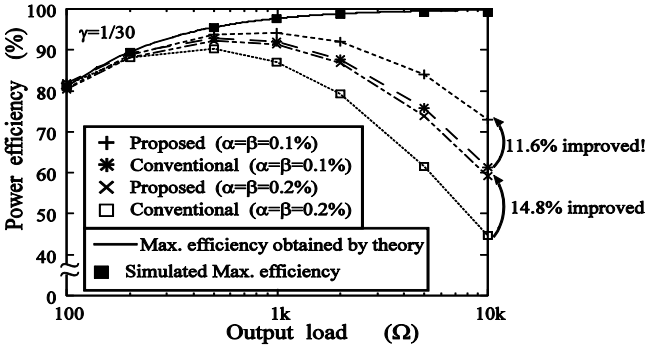
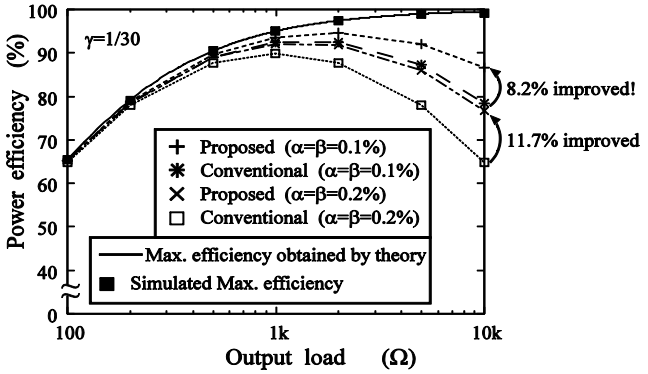


Fig. 7. Proposed ring-type converter in the case of N=3.

Fig. 8 shows the simulated power efficiency as a function of the output load R_L, where the timing of clock pulses was set to as shown in Table II and Table III. In Fig. 8, the solid line shows the maximum power efficiency obtained by theoretical analysis, where the parasitic capacitance was set to zero to evaluate the maximum power efficiency. As Fig. 8 shows, the proposed converter can alleviate the influence of the parasitic capacitance than the conventional converter. Concretely, when the output load R_L is 10kΩ and α=β=0.1% (C_{tj} = C_{bj} = 2pF), the proposed converter can improve the power efficiency more than 8.2%.



(a)



(b)

Fig. 8. Simulated power efficiency as a function of the output load, (a) 2/3x step-down and (b) 3/2x step-up.

TABLE III: Timing of Clock Pulses in the Case of 3/2x Step-Up

3/2x step-up	On	Off
State-T_1	$S_{1,1}$, $S_{2,2}$, $S_{2,3}$, $S_{3,2}$, $S_{4,3}$	Other switches
State-T_2	$S_{5,1}$	Other switches
State-T_3	$S_{1,2}$, $S_{2,3}$, $S_{2,1}$, $S_{3,3}$, $S_{4,1}$	Other switches
State-T_4	$S_{5,2}$	Other switches
State-T_5	$S_{1,3}$, $S_{2,1}$, $S_{2,2}$, $S_{3,1}$, $S_{4,2}$	Other switches
State-T_6	$S_{5,3}$	Other switches

Fig. 9 shows the simulated output voltage as a function of the output load R_L, where the solid line shows the maximum output voltage obtained by theoretical analysis. As Fig. 8 and Fig. 9 show, the theoretical result is in good agreement with the SPICE simulated result. Therefore, the formulas obtained by the theoretical analysis will be helpful to estimate the maximum power efficiency and the maximum output voltage.

Table IV shows the comparison concerning the number of circuit elements. In the point of the circuit topology, the difference between the proposed converter and the conventional converter is only the switch $S_{5,j}$ (j=1,2, …, N), because a parallel-connected structure is not required in the proposed converter. As Table IV shows, the circuit size of the proposed converter is only slightly bigger than that of the conventional converter, because the transistor switch occupies the silicon area much smaller than a capacitor.

TABLE IV: Comparison Concerning the Number of Circuit Elements

Type	Number of switches	Number of capacitors
Proposed converter	15	3
Conventional converter	12	3

Fig. 10 shows the simulated transient characteristic of the output voltage when the output load R_L is 10kΩ. As Fig. 10 shows, the settling time of the proposed converter is almost as same as that of the conventional converter. However, strictly speaking, the settling time of the proposed converter becomes slow due to the time for charge reusing processes.

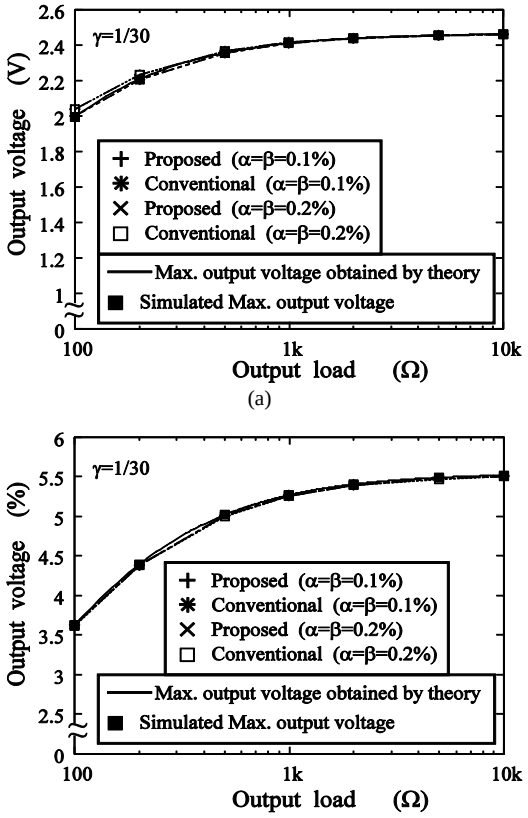


Fig. 9. Simulated output voltage as a function of the output load, (a) 2/3x step-down and (b) 3/2x step-up.

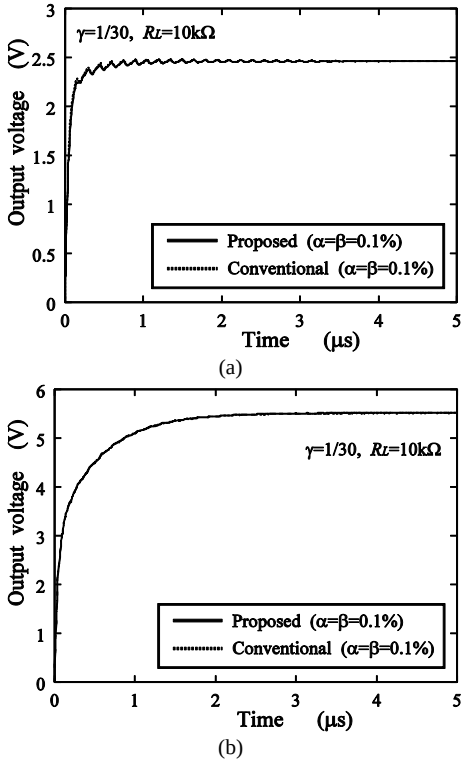


Fig. 10. Simulated transient characteristic of the output voltage, (a) 2/3x step-down and (b) 3/2x step-up.

V. Conclusion

In this paper, a ring-type DC-DC converter using charge reusing techniques has been proposed to improve power efficiency. By connecting stray parasitic capacitances at the end of each clock cycle, the proposed converter can reduce parasitic power losses. The validity of circuit design was confirmed by SPICE simulations and theoretical analysis.

The result of SPICE simulations showed that the proposed converter can reduce the parasitic power losses when the output load R_L is a large value. Concretely, in the case of the 2/3 times step-down conversion, about 11.6% of the power efficiency was improved by the proposed technique when the output load R_L is 10kΩ. On the other hand, in the case of the 3/2 times step-up conversion, about 8.2% of the power efficiency was improved by the proposed technique. Furthermore, concerning the maximum power efficiency and output voltages, the theoretical results are in good agreement with the SPICE simulated results. Therefore, we can estimate the characteristics of the proposed converter by using obtained theoretical equations. The theoretical equation will be helpful to design the proposed converter.

The IC implementation and experimental evaluation of the proposed converter are left to a future study.

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