Influence of Solid State Fault Current Limiter on Grid Connected Photovoltaic System Protection

Jagdish Prasad Sharma and H. Ravishankar Kamath

***Abstract*—Distributed generation (DG) are connected to the grid via a power electronic interface that regulates the amount of power injection to the grid by regulating point of coupling (PCC) voltage or converter control circuit. The PCC parameters are used to decide the operational mode of DG. The power electronic interface badly affected by at current and voltage in the event of a fault. The focus of this paper is at describing how solid-state fault current limiter (SSFCL) may be considered for voltage sag mitigation and fault current control of a parallel distribution feeder connected to a 100 KW photovoltaic system. This 100 KW photovoltaic system is connected to above said feeder with a 100 KVA transformer. To avoid any damage to power electronic interface, it is required to determine prospective fault current and voltage sag mitigation at point of coupling (PCC). The performance of SSFCL is assessed with prospective fault current, voltage sag mitigation and suppression of fault current for unsymmetrical /symmetrical faults on a parallel distribution feeder connected to photovoltaic system.**

***Index Terms*—Voltage sag mitigation, solid-state fault current limiter, prospective fault current, grid connected photovoltaic.**

I. Introduction

Voltage sags and prospective fault current are considered an important aspect to operate power electronic interfaces connected at PCC. The PCC parameters are utilized to control converter circuit independently. It is common practice to isolate DG in case of fault as it lead may grid instability. Most of distribution feeder has overhead configuration and subjected to vehicle collisions, dust deposition on insulator and lightning.

So, it is needful to protect the power electronic interfaces against voltage imbalance, voltage sags, prospective fault current, fault current and interruption, etc., under abnormal condition. The state fault current limiter (SSFCL) has good performance in terms of fault current limiting capacity, restoration time and voltage sag mitigation for a distribution feeder.

This paper utilizes the developed SSFCL model [1] to investigate the effect of unsymmetrical /symmetrical faults on power electronics interface. The impact of this SSFCL at five different firing angle in terms of prospective fault current and voltage sag mitigation investigated [2].

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S. Noman ud Din, B. Islam and S. Ahmed demonstrated a superconducting fault current limiter placed in a strategic manner to suppress fault current and stability enhancement of a solar integrated power system [3]. As DG integration raises the fault level of existing system and affects protective device operations. In this regard an experimental setup was designed and analyzed the impact of DG integration of coordination between protective devices by S. H. Lim and J. C. Kim [4]. The power electronic interface components are vulnerable to voltage dip. S. B. Naderi *et al*., improved low voltage ride-through (LVRT) capability of the inverter and investigate its performance for both symmetrical and asymmetrical faults [5]. A correction in a protection coordination scheme demonstrated for DG connected feeder [6]. S. Farhadkhani *et al*., investigated the effect of the superconducting, solid state and hybrid types fault current limiters (FCLs) on IEEE 34 node test feeder in presence of wind turbine induction generators [7]. M. Alex and A. A. Josephine analyzed the impact the role of dispersed generations location on protective devices Co ordination [8]. R. Elavarasi , and P. Saravanan investigated the performance of a solid state fault current limiter (SSFCL) on wind power integrated distribution system [9].

To limit voltage sag and phase jumps at PCC during fault commencement, a new fault current limiter presented and validate through the experimental setup [10]. In this paper, a test system mentioned is utilized with the assumption of constant impedance load [10]. A 100 KW photovoltaic array with slight modification is considered as a DG unit for the above test system and performance assessed with prospective fault current, voltage sag mitigation and suppression of fault current for unsymmetrical /symmetrical faults.

II. Test System

This paper has been discussed voltage sag mitigation and suppression of fault current for unsymmetrical /symmetrical faults in a test system have two parallel feeders as shown in Fig. 1 [6].

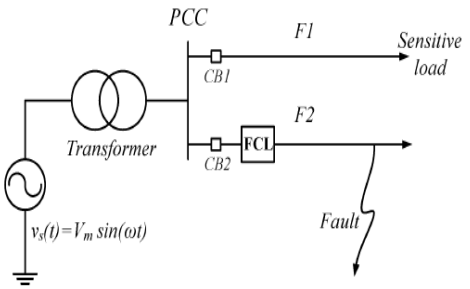

Fig. 1. Single-line diagram of test feeder.

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A. Simulink Model of Test System

The F1 and F2 feeder have a constant impedance load, whereas original test system considered F1 feeder load as constant impedance load. Different fault created at load end of F2 feeder, which resulted in reduction of common points of coupling (PCC) and load terminal with the increased transformer current. The simulink model of this test system is shown in Fig. 2. A 100 KW PV system is integrated at PCC of test system [6].

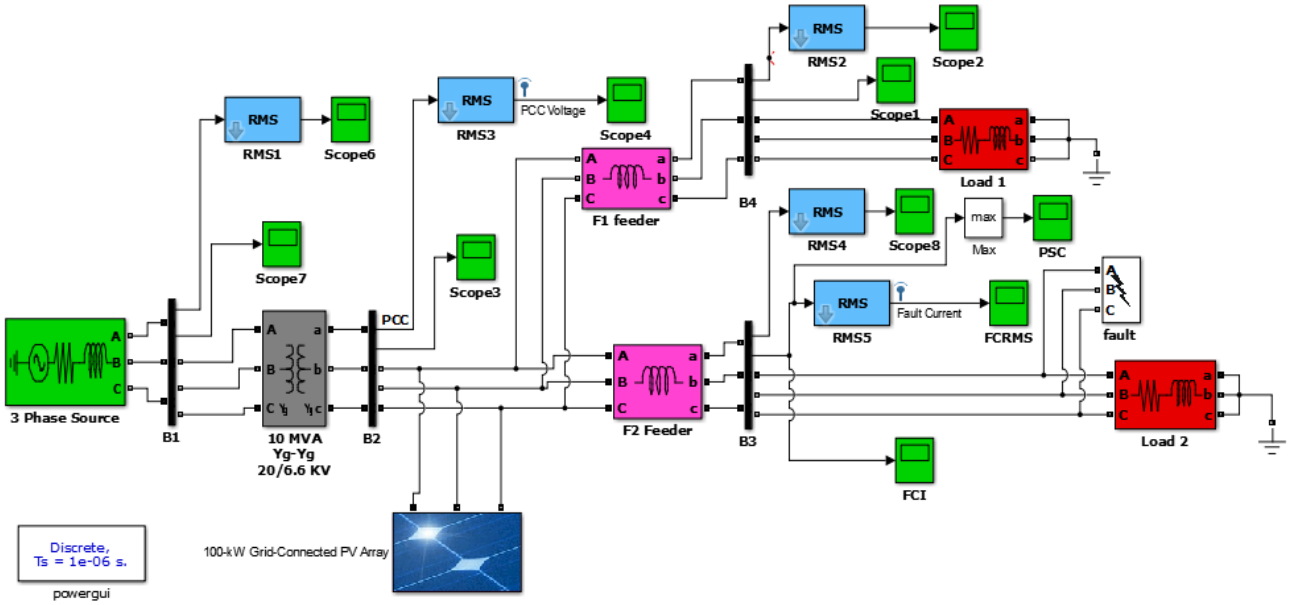


Fig. 2. Simulink model of test system.

B. Solid State Fault Current Limiter

A solid-state fault current limiter (SSFCL) utilized for voltage sag mitigation and fault current control in this work. The basic topologies of solid-state fault current limiters are as under

- Series switch type,
- Bridge type and
- Resonant type.

In this paper, we have utilized series switch type with inductor, which is inserted in series with a circuit. This series switch type SSFCL are composed of three parallel circuits as shown in Fig. 4. In case of fault the current path is diverted from Thyristor branch 1 to Thyristor branch 2 and overvoltage absorption implemented with the help of surge arrester and associated snubber circuit with thyristor branches.

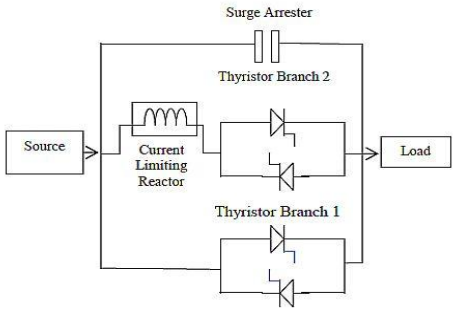


Fig. 3. Basic topology of SSFCL.

Control and current limiter model for above solid state fault current limiter (SSFCL) simulated by using topology as shown in Fig. 3 [1].The control block has two individual synchronized 6 pulse generators for Thyristor branch 1 and Thyristor branch 2, which are fired at 10^0. In this block current is continuously watched and compared with preset value of current. In this paper, we have considered the fault current at 111 Ampere, which is 15% more of nominal value for the concerned branch. Apart from, above we have taken fault current limiting inductor as 10mH.

C. Grid Connected Photovoltaic System

This paper examines how is affected by the power electronics interface of a solar photovoltaic (PV) system affected by voltage sag and prospective fault current. The PV array operating at standard test conditions, 25 ℃, 1000 W/m^2 solar irradiance. The PV array makes is Sun power SPR-305-WHT with 66 parallel strings and each string has 5 modules in series. A 100-kVA 260V/6.6 KV three-phase coupling transformer is utilized to synchronize this 100 KW photovoltaic system with test system. The parameters for PV distributed generation parameters are listed in Table I.

TABLE I: PHOTOVOLTAIC PARAMETERS

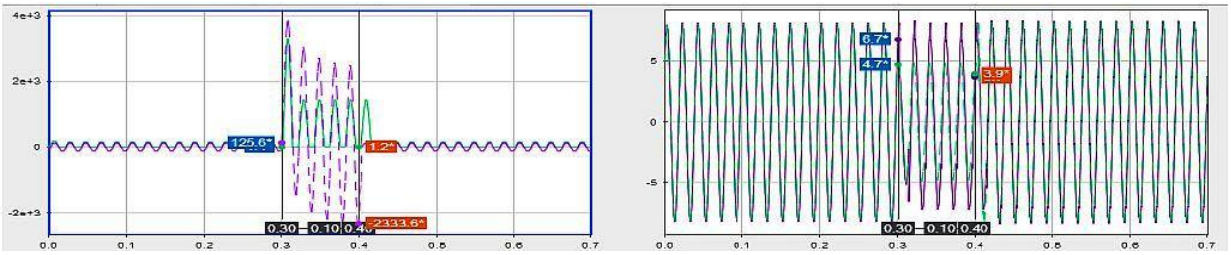
Component	Parameters
DC to DC Converter and MPPT Control	
Initial duty cycle, PWM switching frequency	0.5, 5000 HZ
DC to DC converter resistance and inductance	5mΩ, 5mH
MPPT control time, Initial duty cycle	200 µsec,0.5
Voltage source converter	
VSC input side capacitance, IGBT resistance	125mF , 0.2mΩ
VSC snubber resistance and capacitance Cs	1MΩ, infinite
Nominal DC bus voltage, Choke impedance	450 V, 2 mΩ and 250 µH
Grid side transformer (Star/Delta)	
Nominal KVA and frequency	100 KVA, 60 HZ
Per unit resistance and reactance	0.01,0.03
Nominal line HV and LV side voltage (rms)	6.6 KV, 260V
Grid side inductor resistance and inductance	1mΩ, 45µH
Star grounded capacitor bank	260V,10 KVAR, 60 HZ
Per unit resistance and reactance	0.01,0.03

III. Simulation Result

The performance of SSFCL evaluated in terms of Voltage sag mitigation at point of coupling (PCC), fault current suppression, power injected by photovoltaic system. Following fault scenarios is created on bus 3.

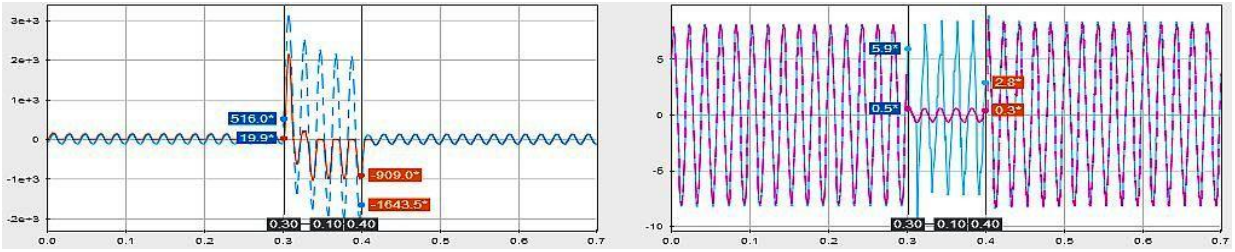
- Line to ground fault-Phase A to ground
- Double line fault-Phase A and B
- Double line to ground fault-Phase A and B with ground
- Triple line to ground fault-Phase A, B and C with ground

The Simulink solver parameters are variable step type with ode23tb, 1e-6 relative tolerance, 1e-1 absolute error, and simulation time 0.6 seconds. As phase A is common for all fault scenarios, therefore we depicted voltage and fault current for phase A in "Fig. 4, Fig. 5, Fig. 6, Fig. 7". All dotted lines represent the parameters without SSFCL integration.



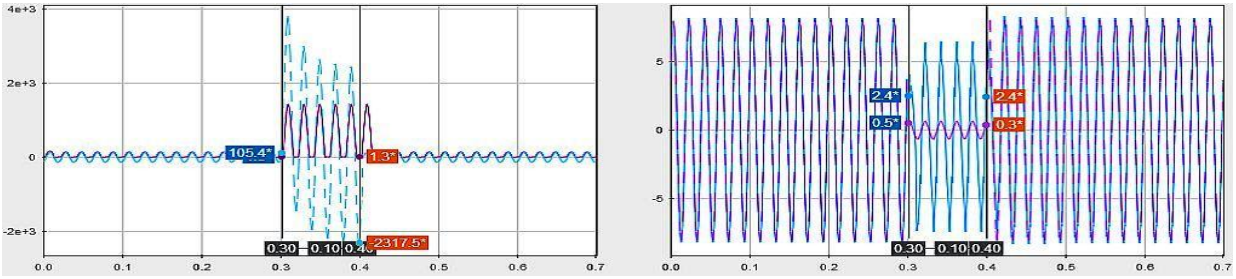
(a) Fault Crurent-Bus 3 (b) PCC Voltage-Phase A

Fig. 4. Impact of SSFCL on various parameters for LG.



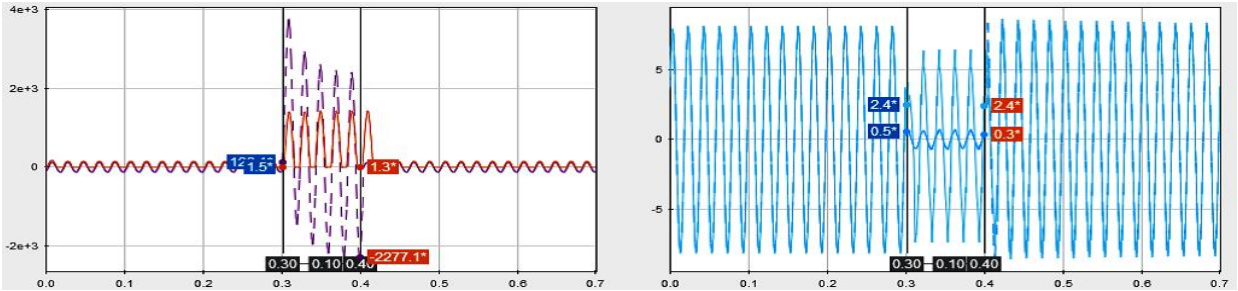
(a) Fault Current-Bus 3 (b) PCC Voltage-Phase A

Fig. 5. Impact of SSFCL on various parameters for LL.



(a) Fault Current-Bus 3 (b) PCC Voltage-Phase A

Fig. 6. Impact of SSFCL on various parameters for LLG.



(a) Fault Current-Bus 3 (b) PCC Voltage-Phase A

Fig. 7. Impact of SSFCL on various parameters for LLLG.

The effectiveness of SSFCL in the presence of a PV distribution system investigated and its performance was compared without SSFCL. It is observed that for all said fault scenarios; SSFCL has reduced the prospective fault current through bus 3 significantly. This will reduce protection system augmentation/renovation cost. It is also observed that SSFCL has shown the ability to keep almost constant real power flow of PV system under faulty conditions. Thus SSFCL is a considerable approach for low/medium voltage network to optimum existing asset utilization with enhancement of network flexibility, sustainability, and reliability. Voltage sags mitigation, and fast post-fault recovery voltage at PCC makes SSFCL more suitable for DG integration for low/medium voltage network. Thus, it is clear

that SSFCL is mitigating voltage and diminishing line fault current significantly.

IV. Conclusion

In this paper a state fault current limiter (SSFCL) utilized to protect power electronic interface of a 100 KW photovoltaic system. This PV system, is a connected to a parallel distribution feeder connected to a 100 KW photovoltaic system. Under abnormal condition, this SSFCL worked efficiently to voltage sag mitigation and fault current suppression aspects. Thus SSFCL is a viable option over conventional solutions for making secure and qualitative power supply injection of the PV system to the distribution grid.

References

[1] J. P. Sharma and V. Chauhan, "Application of solid state fault current limiter on express feeder for voltage sag mitigation," in *Proc. IEEE International Conference on Computational Intelligence and Computing Research (ICCIC)*, Coimbatore, 2014, pp. 1-4.

[2] J. P. Sharma and V. Chauhan, "Analysis and control of fault current by firing angle control of solid state fault current limiter," in *Proc. IEEE International Conference on Energy Systems and Applications*, Pune, 2015, pp. 527-530.

[3] S. N. U. Din, B. Islam, and S. Ahmed, "Optimal positioning of bridge type superconducting fault current limiter in solar integrated electric power grid," in *Proc. Symposium on Recent Advances in Electrical Engineering (RAEE)*, Islamabad, 2015, pp. 1-6.

[4] S. H. Lim and J. C. Kim, "Analysis on protection coordination of protective devices with a SFCL due to the application location of a dispersed generation in a power distribution system," *IEEE Transactions on Applied Superconductivity*, vol. 22, no. 3, pp. 5601104-5601104, 2012.

[5] S. B. Naderi, M. Negnevitsky, A. Jalilian, M. T. Hagh, and K. M. Muttaqi, "Voltage sag compensation of point of common coupling for low voltage ride-through enhancement of inverter interfaced DG using bridge type FCL," in *Proc. Power Engineering Conference (AUPEC)*, 2015 Australasian Universities, Wollongong, pp. 1-6, 2015.

[6] S. H. Lim, J. S. Kim, and J. C. Kim, "Study on Correction of Protective Devices for Application of a SFCL in a Power Distribution System With a Dispersed Generation," *IEEE Transactions on Applied Superconductivity*, vol. 23, no. 3, pp. 5603504-5603504, June 2013.

[7] S. Farhadkhani, J. Lobry, F. Vallée, and O. Durieux, "Investigating the characteristics and effects of FCLs on distribution grids with wind generation," in *Proc. Electrical Power and Energy Conference (EPEC)*, IEEE, Calgary, AB, 2014, pp. 65-70.

[8] M. Alex and A. A. Josephine, "Impact due to the application Location of a Dispersed generation on the distribution system Protection with SFCL Application Using PSCAD," in *Proc. International Conference on Energy Efficient Technologies for Sustainability (ICEETS)*, Nagercoil, 2013, pp. 1225-1229.

[9] R. Elavarasi and P. Saravanan, "Impact of distributed generation on distribution systems and its protection," *Indian Journal of Science and Technology*, vol. 57, pp. 85-90, November 2014.

[10] M. Jafari, S. B. Naderi, M. T. Hagh, M. Abapour, and S. H. Hosseini, "Voltage sag compensation of point of common coupling (PCC) using fault current limiter," *IEEE Transactions on Power Delivery*, vol. 26, no. 4, pp. 2638-2646, Oct. 2011.

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